REMARKS

Applicants and their representative, Mr. Frank Occhiuti, wish to thank Examiner Chu for the helpful and courteous interview conducted on August 11, 2004. We agree with the Examiner's description of the substance of the interview as set forth in the Interview Summary form (PTOL-413) provided by Examiner Chu at the end of the interview.

We acknowledge the Examiner's indication that dependent claims 6 and 10 would be allowable if amended to be in independent form and to include all of the features recited in the base and any intervening claims. We have also amended claims 1-10. These amendments are supported by applicants' specification at page 13, lines 14-28 (Paragraphs [0043] and [0044]) and page 18, line 31 to page 19, line 15 (Paragraphs [0059] and [0060]).

Prior Art Rejections

Claims 1 and 2 were rejected as being unpatentable over Willis (U.S. Patent 6,693,857) in view of Arataki et al. (U.S. Patent No. 5,831,955 "hereinafter Arataki). Applicant traverses this rejection. Applicant traverses this rejection.

Independent Claim 1

We submit however that Willis does not disclose a data recorder including among other features a retry determination circuit for determining whether an address of written data, which is read from a recording medium, and an address of read data, which is provided to an encoder from a buffer memory, are the same and 2) a second retry determination circuit for determining whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same, as recited in amended claim 1. Indeed, Willis says nothing about his circuit determining whether addresses or timings are the same. Rather, Willis discloses data buffer management and a method for assigning record segments and play back recorded segments on a disk after a pause.

Arataki also does not disclose a data recorder including, among other features, first and second retry determination circuits as recited in amended claim 1. In particular, like Willis,

Arataki does not disclose a circuit that determines whether addresses or timings are the same. Rather, Arataki discloses a technique for improving the operation stability of a disk recording system with jitter free.

We further submit that because claim 2 depends from independent claim 1, claim 2 is patentable for at least the same reason that claim 1 is patentable.

The Examiner also rejected claims 3-5 and 7-9 as being unpatentable over Willis in view of Arataki.

Independent Claim 3

Willis does not disclose a data recorder including among other features 1) a first retry determination circuit for determining whether an address of written data, which is read from a recording medium, and a write data address, which is stored in one or more address memories, are the same, and for determining whether an address of read data, which is provided to an encoder from a buffer memory, and a read data address, which is stored in the one or more address memories, are the same and 2) a second retry determination circuit for determining whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same. As discussed above, Willis does not disclose a circuit that determines whether addresses or timings are the same.

Arataki does not disclose the first retry determination circuit and the second retry determination circuit recited in independent claim 3. As discussed above, Arataki does not disclose a circuit whether addresses or timings are the same.

We further submit that because claims 4-6 depend from independent claim 3, these dependent claims are patentable for at least the same reasons that claim 3 is patentable.

Independent Claim 7

Willis does not disclose a data recorder including among other features 1) a retry determination circuit for determining whether an address of written data, which is read from a

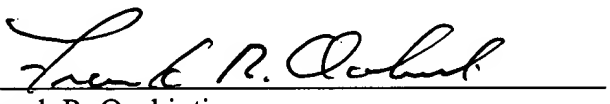
recording medium, and a write data address, which is stored in one or more address memories, are the same, and for determining whether an address of read data, which is provided to an encoder from a buffer memory, and a read data address, which is stored in the one or more address memories, are the same and 2) a synchronizing circuit that determines whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same. As was the case with independent claims 1 and 3, neither Willis nor Arataki disclose a retry determination circuit that determines whether addresses or timings are the same.

We further submit that because claims 8-10 depend from independent claim 7, these dependent claims are patentable for at least the same reasons that claim 7 is patentable.

Enclosed is a $450.00 check for the Petition for Extension of Time fee (2 months, large entity). Please apply any other charges or credits to deposit account 06-1050, referencing Attorney Docket Number 10449-033001.

Respectfully submitted,

Date: December 29, 2004



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